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The effect of porous structure of PMMA tunneling dielectric layer on the performance of nonvolatile floating-gate organic field-effect transistor memory devices

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ABSTRACT

In this paper, we used the low and high density porous structure of polymethylmethacrylate (PMMA) film as tunneling dielectric layer in the floating-gate organic field-effect transistor (OFET) memory devices. Compared to the thin/thick nonporous structure of PMMA tunneling layer, the porous structure of PMMA tunneling layer had positive impacts on the device performance of the floating-gate OFET memory devices. Moreover, it was found that the memory performance was also increased as pore density of PMMA film increased. The atomic force microscopy (AFM) results of both porous structure of PMMA film and pentacene film on porous structure of PMMA film revealed that high density porous structure of PMMA tunneling layer can produce larger tunneling area and more electron transfer paths between pentacene film and PMMA film, which resulted in high electron capture and release efficiency of the floating-gate OFET memory devices with porous structure of PMMA tunneling layer. In addition, our porous structure of PMMA tunneling layer as well as nonporous PMMA film has high electrical insulating property due to their semi-hollow structure film, which is favourable to maintain stable retention property. Eventually, the floating-gate OFET memory devices with high density porous structure of PMMA tunneling layer showed good nonvolatile memory properties with a large memory window of about 43 V, a high ON/OFF current ratio of about 10^4, and stable endurance and retention properties. Our results provided a new strategy to achieve the high performance floating-gate OFET memory devices.

1. Introduction

Organic optoelectronic devices have attracted extensive attention due to their excellent properties such as low cost, flexibility and low temperature processing [1–4]. Considerable attempts have been devoted to the developments of organic electronics such as organic light-emitting diodes (OLEDs), organic field-effect transistors (OFETs) and organic photovoltaic cells (OPVs) and so on [1,5–7]. Among them, nonvolatile organic memory devices based on organic field-effect transistors are generally expected to be the promising candidates for the next generation memories, owing to their high storage density, nondestructive read-out, easily integrated structure and well compatibility with complementary oxide semiconductor (CMOS) [8–11]. As one of important organic field-effect transistor memory devices, floating-gate OFET memory devices have advantages in the reliable data retention and endurance because the floating gate is completely isolated by the blocking dielectric layer and the tunneling dielectric layer [12–14]. For the floating-gate OFET memory devices, their memory performance is

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closely related to both the floating-gate layer and the tunneling dielectric layer [15,16]. Many efforts have been devoted to optimizing the floating-gate layers, different types of materials including inorganic materials, organic molecules and polymers, and metallic nanoparticle have been demonstrated to act as charge storage media, which effectively enhances the nonvolatile memory properties of floating-gate OFET memory devices [17–23]. Besides the floating-gate layers, the tunneling dielectric layer also has a direct impact on memory performance of floating-gate OFET memory devices [24,25]. When the film thickness of the tunneling dielectric layer is thicker, the capture and release efficiency of the charge between the conductive channel and floating-gate layer is reduced, which causes the high programming/erasing voltage and poor endurance property. When the film thickness of tunneling dielectric layer is thinner, the charge can be easily released from floating-gate layer to the conductive channel, which causes the poor retention property [26–28]. In addition, the surface morphology of the tunneling dielectric layer also can't cause damage to the mobility of OFETs, which ensures high device performances [29,30]. In view of the above facts, the high quality tunneling dielectric layer is also required to achieve high performance of floating-gate OFET memory devices [31,32].

In this paper, we fabricated the floating-gate OFET memory devices using the thin/thick nonporous and low/high density porous structure of PMMA film as tunneling layer and discrete distribution gold nanoparticles (Au-NPs) as the floating-gate layer, respectively. The memory properties of the four floating-gate OFET memory devices were investigated. According to the comparison results, it was found that the porous structure of PMMA tunneling layer had both the high electron capture and release efficiency and high electrical insulating property, which had positive impacts on device performance. As pore density of PMMA tunneling layer increased, the device performance of the floating-gate OFET memory devices was also increased. And finally, the corresponding mechanisms of the porous structure of PMMA tunneling layer on the capture and release process of the charge in the floating-gate OFET memory devices were detailedly discussed.

2. Experimental

Fig. 1(a) shows the schematic illustration of the floating-gate OFET memory devices with the porous structure of PMMA tunneling layer. These devices were fabricated on heavily doped n-type Si wafer using 300 nm thermally SiO_2 which served as the gate electrode and the gate blocking layer, respectively. The Si/SiO_2 substrate was cleaned sequentially in an ultrasonic bath with acetone and isopropanol for 5 min each, and then dried in the oven at 100 °C for 30 min after rinsing with deionized water. The gold nanoparticles (Au-NPs) were decorated on the SiO_2/Si substrate by drop coating with gold colloid to form floating-gate layer, followed by baking at 100 °C for 10 min to evaporate the solvent, and the scanning electron microscope images (SEM) of Au-NPs floating layer was shown in Fig. 1(b). The low and high density porous structure of PMMA film was prepared on the substrate via spin-coating process at 2000 rpm for 30s using a 10 mg/ml and 20 mg/ml solution in tetrahydrofuran (THF) and H_2O (THF: H_2O = 100:5, v/v), respectively, which was acted as the tunneling dielectric layer, and their AFM images were shown in Fig. 1(c) and (d), respectively. In addition, the thick and thin nonporous structure of PMMA film was also prepared via spin-coating process at 3000 rpm for 30s using a 10 mg/ml and 5 mg/ml solution in THF, respectively, and their AFM images were shown in Fig. 1(e) and (f). Subsequently, the substrate was transferred to the oven to bake for 20 min at 120 °C in air. After that, the semiconductor layer of 50 nm thick pentacene was deposited onto the substrate by the thermal vacuum evaporation method at a deposition rate of 0.1 Å/s and at a pressure of 5×10^{-4} Pa, which was the active layer. Finally, about 60 nm thick copper (Cu) as source and drain electrodes was thermally evaporated through a shadow mask with the channel width (W = 2000 μm) and the channel length (L = 100 μm) to complete the top-contact and bottom-gate floating-gate OFET memory devices. The electrical characteristics of the memory devices were characterized using an Agilent B1500A semiconductor parameter analyzer. All electrical measurements were carried out under ambient conditions at room temperature.

3. Results and discussions

Fig. 2 shows the representative output and transfer characteristics of the floating-gate OFET memory devices with high density porous structure of PMMA tunneling layer. The typical p-type field-effect transistor behavior with good saturation property was observed, the field-effect mobility (μ), threshold voltage (V_{TH}) and ON/OFF current ratio was calculated to be 0.49 $cm^2 V^{-1}s^{-1}$, −11 V and 10^5, respectively, as shown in Table 1. In addition, the field-effect properties of the floating-gate OFET memory devices with thin/thick nonporous and low density porous structure of PMMA tunneling layer were also characterized, and their electrical parameters of these devices were summarized in Table 1. It can be seen that the field-effect parameters of OFETs with porous structure of PMMA tunneling layer was comparable to that of OFETs with thick nonporous structure of PMMA tunneling layer, demonstrating that the porous structure of PMMA film did not have a negative impact on field-effect performance of the floating-gate OFET memory devices, which was crucial for OFET memory devices to achieve stable memory properties. The higher μ of the floating-gate OFET memory devices with high density porous structure of PMMA tunneling layer may be related to the growth mode of pentacene film on porous PMMA film. The AFM images of pentacene film grown on nonporous and porous PMMA film were characterized, as shown in Fig. S1. It can be seen that most pentacene grains which composed of pentacene films grown on nonporous PMMA film was discrete, which hindered the transport of the carriers in the conductive channel of OFETs. Although the porous structure was observed in the pentacene film grown on porous PMMA film, the growth of their pentacene grains was continuous, which was favourable for the transport of the carrier in the conductive channel of OFETs. In addition, as shown in Fig. 1(d), the pore diameter of high density porous PMMA film was about 55 nm, moreover, the pore distribution in the PMMA film was not very dense, thus the pores of high density porous PMMA film couldn't cause harm to the growth of pentacene film. The above two facts may be the reason for the higher mobility of OFETs with high density porous structure of PMMA tunneling layer.

To investigate the impact of the thin/thick nonporous and low/high density porous structure of PMMA film as tunneling layer on the memory properties of the floating-gate OFET memory devices, the typical shift in the transfer curve of the OFET memory devices with thin/thick nonporous and low/high porous structure of PMMA tunneling layer was measured, as shown in Fig. 3. The initial position of the transfer curve was defined as initial state for the OFET memory devices. When the programming voltage of 80 V was applied to four memory devices for 3 s in the light conditions, the transfer curves of four memory devices all shifted toward the positive direction and steadily sustained at the shifted position even after the power supply was removed, showing that the charge in the conductive channel can pass through the nonporous and porous structure of PMMA tunneling layer and further be captured by Au-NPs floating layer. The shifted process and position of the transfer curve was defined as programming process and

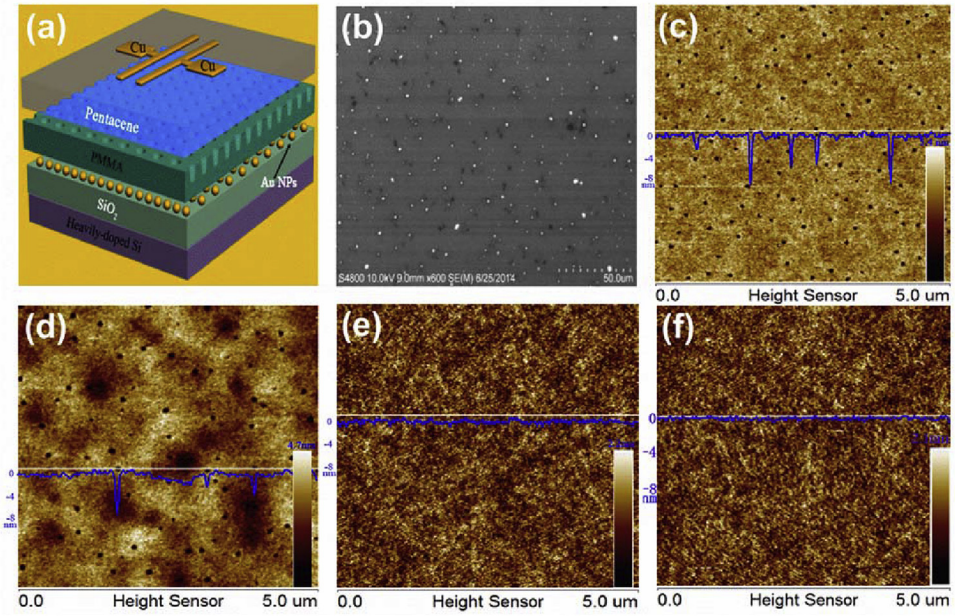

Fig. 1. (a) The schematic illustration of the floating-gate OFET memory devices with the porous structure of PMMA tunneling layer. (b) The SEM images of Au-NPs floating layer. The AFM images of (c) high density and (d) low density porous and (e) thick nonporous and (f) thin nonporous structure of PMMA film.

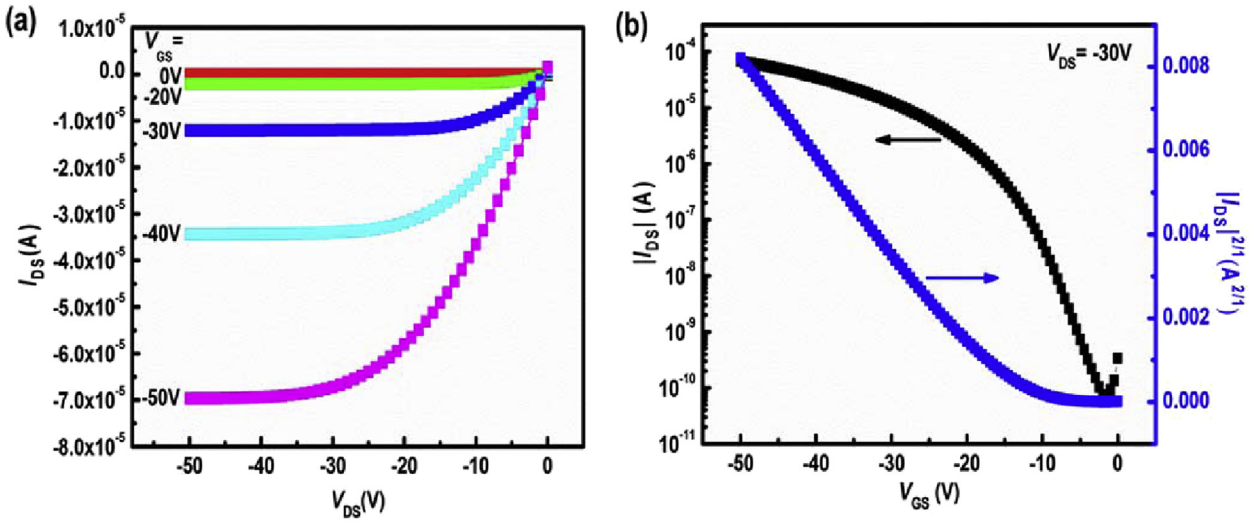

Fig. 2. The representative (a) output and (b) transfer characteristics of the floating-gate OFET memory devices with high density porous structure of PMMA tunneling layer.

Table 1
The memory parameters of the four floating-gate OFET memory devices with thin/thick nonporous and low/high density porous structure of PMMA tunneling layer.

Devices	Pore density	Thickness/nm	Mobility/$cm^2V^{-1}S^{-1}$	On/off current ratio	Threshold voltage/V	Memory window/V	$\Delta n/cm^{-2}$
A	High	26	0.49	10^5	−5	43	2.87×10^{13}
B	Low	28	0.31	10^5	0	35	2.34×10^{13}
C	Nonporous	23	0.33	10^5	−10	30	2.00×10^{13}
D	Nonporous	12	0.64	10^5	−7	36	2.40×10^{13}

programmed state for OFET memory devices, respectively. The positive shift of transfer curve during the programming process showed that the type of captured charge by Au-NPs floating layer was electron [33]. In addition, the relationship between the light illumination time and memory effect was as shown in Fig. S2. It was found that the shifts in the transfer curve of the floating-gate OFET memory devices with the high density porous structure of PMMA tunneling layer were also proportionally increased as the light illumination time increased from 1 s to 3 s, however, it couldn't further shifted toward the positive direction when the light illumination time was 5 s. Subsequently, the four memory devices were applied to the erasing voltage of −150 V for 3 s in the dark, and the transfer curve shifted in the negative direction, which was defined as erasing process and erased state, respectively. It can be

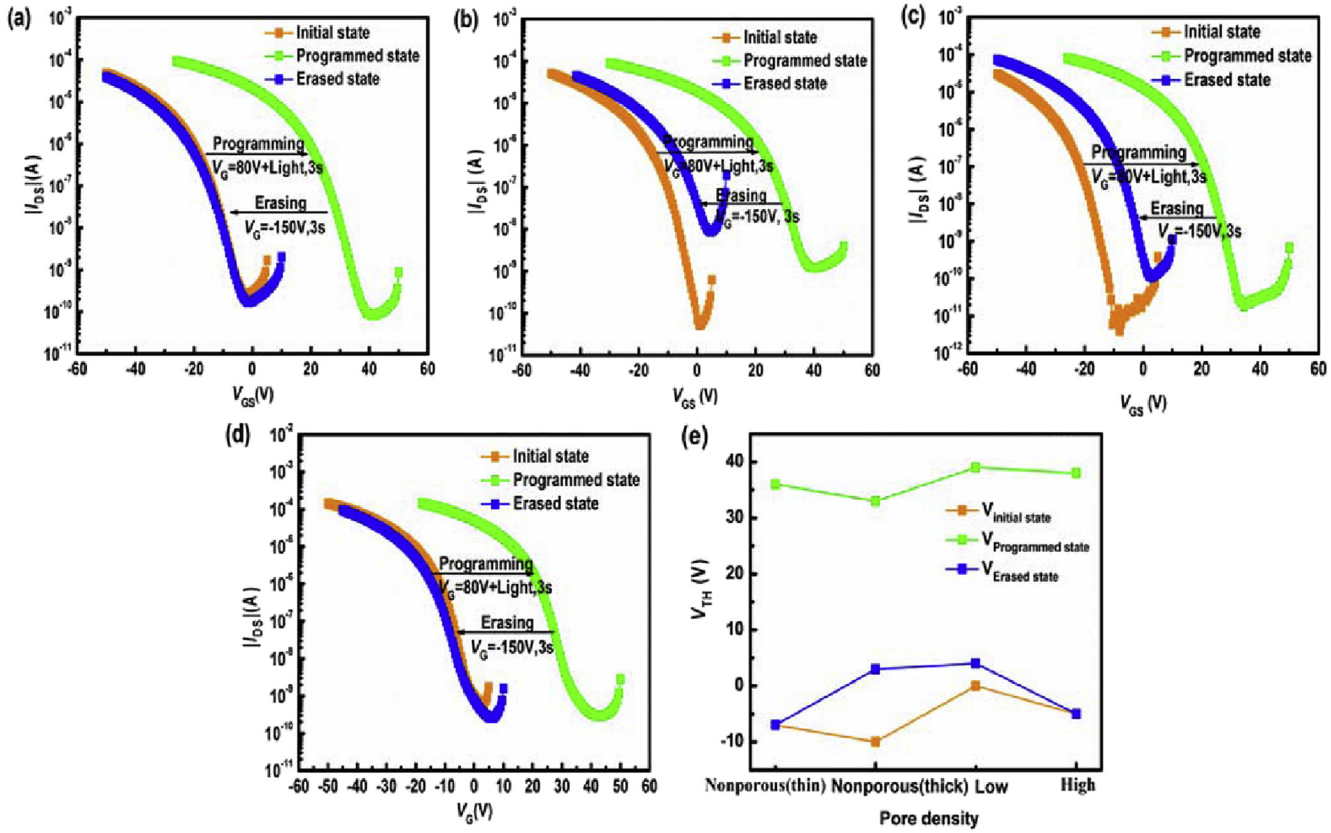

Fig. 3. The programming and erasing characteristics of the floating-gate OFET memory devices with (a) high density and (b) low density porous and (c) thick and (d) thin nonporous structure of PMMA tunneling layer. (e) The shift of V_{TH} as a function of the four floating-gate OFET memory devices under the same programming/erasing voltage.

seen that the transfer curve of the floating-gate OFET memory devices with thin nonporous and high density porous structure of PMMA tunneling layer could completely recovered to the initial state, as shown in Fig. 3(a) and (d), respectively, showing that the captured electrons by Au-NPs floating layer could be completely released into the conductive channel through the thin nonporous and the high density porous structure of PMMA tunneling layer. However, the transfer curve of the floating-gate OFET memory devices with thick nonporous and low density porous structure of PMMA tunneling layer did not completely recovered to the initial state, as shown in Fig. 3(b) and (c), respectively, showing that the captured electrons by Au-NPs floating layer could not be completely released to the conductive channel through the thick nonporous and the low density porous structure of PMMA tunneling layer under the same erasing voltage. Although the four memory devices all showed programming and erasing characteristics, the shift of V_{TH} as a function of thin/thick nonporous and low/high density porous structure of PMMA tunneling layer under the same programming/erasing operation conditions was different, as shown in Fig. 3(e). It can be seen that it was easier for V_{TH} of erased state of the floating-gate OFET memory devices to recover to their initial state with the increasing of pore density of PMMA film except that of memory devices with thin nonporous structure of PMMA tunneling layer, meaning that more captured electrons by Au-NPs floating layer can be released into the conductive channel through the porous structure of PMMA tunneling layer as pore density of PMMA film increased. For the floating-gate OFET memory devices, the thin tunneling layer is usually favourable to enhance the capture and release efficiency of the charge. The above erasing process demonstrated that although the its thickness was thick, the high density porous structure of PMMA film as well as thin nonporous structure of PMMA film is also favourable to sufficiently release the captured electrons by Au-NPs floating layer during the erasing process, which is critical for achieving high performance floating-gate OFET memory devices.

The number of captured electrons (Δn) was roughly calculated according to the following equation:

$$\Delta n = \frac{\Delta V_{TH}}{e} C_i$$

where e is the element charge, ΔV_{TH} is the shift of threshold voltage and C_i is the capacitance of the gate dielectric [34]. According to the equation, the Δn of the four floating-gate OFET memory devices with thin/thick nonporous and low/high porous structure of PMMA tunneling layer was about 2.40 × 10^{13} cm^2, 2.00 × 10^{13} cm^2, 2.34 × 10^{13} cm^2 and 2.87 × 10^{13} cm^2, respectively, which was summarized in Table 1. The results showed that the porous structure of PMMA tunneling layer can promote the number of electrons captured by Au-NPs floating layer during the programming process when the thickness of PMMA tunneling layer of the floating-gate OFET memory devices was kept identical. As mentioned above, the porous structure of PMMA tunneling layer can also sufficiently release the trapped electrons by Au-NPs floating layer during the erasing process. Eventually, the memory window became larger as pore density of PMMA film increased, and the largest memory window of 43 V was observed in the floating-gate OFET memory devices with high density porous structure of PMMA tunneling layer, as shown in Table 1. However, it should be noted that although the memory window of the floating-gate OFET memory devices with thin nonporous structure of PMMA tunneling layer was larger than that of the floating-gate OFET memory devices with

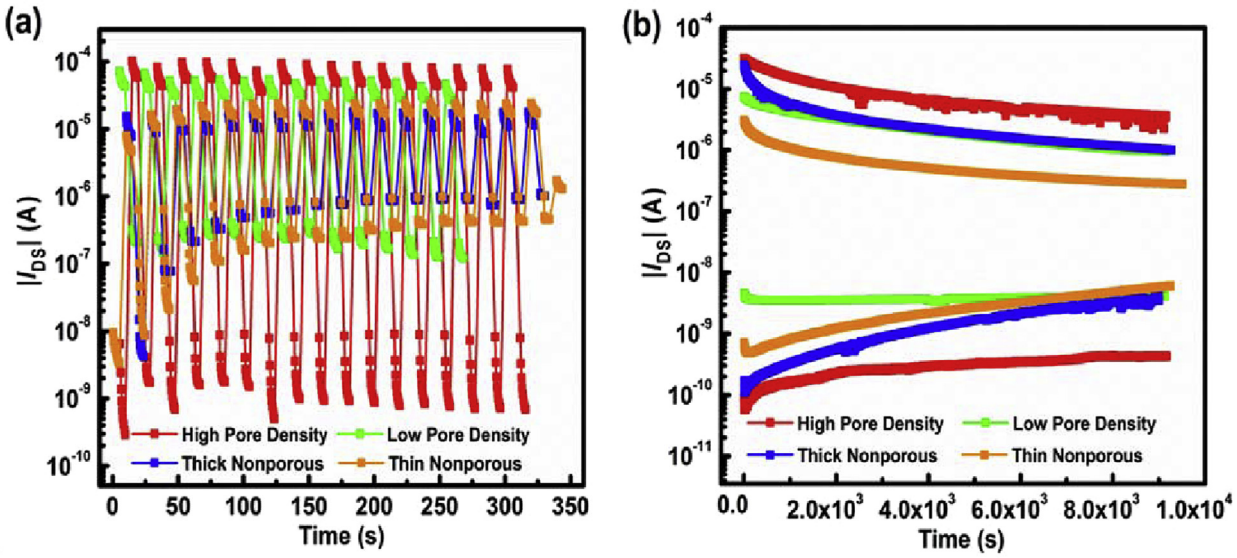

Fig. 4. (a) The endurance and (b) the retention characteristics of the four floating-gate OFET memory devices with thin/thick nonporous and low/high density porous structure of PMMA tunneling layer.

thick nonporous and low density porous structure of PMMA tunneling layer, it was still lower than that of the floating-gate OFET memory devices with high density structure of PMMA tunneling layer. Therefore, the high density porous structure of PMMA film as tunneling layer can effectively enhance the capture and release efficiency of electrons between the conductive channel and Au-NPs floating layer, which can result in the large memory window of the floating-gate OFET memory devices.

Fig. 4(a) showed the endurance characteristics of the floating-gate OFET memory devices with thin/thick nonporous and low/high density porous structure of PMMA tunneling layer with a series of programming ($V_G = 80$ V, light illumination for 3 s), reading ($V_G = 0$ V, in the dark), and erasing ($V_G = -150$ V, in the dark) processes. It can be seen that the floating-gate OFET memory devices with high density porous PMMA tunneling layer showed stable programmed state and erased state, and the ON/OFF current ratio was over 10^4 during the endurance testing process. For the floating-gate OFET memory devices with low density porous PMMA tunneling layer, although both programmed state and erased state were also stable, the ON/OFF current ratio was only 10^2. For the floating-gate OFET memory devices with thin/thick nonporous PMMA tunneling layer, the I_{DS} values at the erased state gradually increased during the endurance testing process, which resulted in the reduction of ON/OFF current ratio from 10^3 to 10. Fig. 4(b) showed the retention characteristics of the floating-gate OFET memory devices with thin/thick nonporous and low/high density porous structure of PMMA tunneling layer. Compared to the thin/thick nonporous structure of PMMA tunneling layer, the floating-gate OFET memory devices with low and high density porous structure of PMMA tunneling layer showed stable retention characteristics, and high ON/OFF current ratio of about 10^4 can be maintained in the floating-gate OFET memory devices with high density porous structure of PMMA tunneling layer during the retention time. Therefore, the high density porous structure of PMMA film as tunneling layer could effectively improve endurance and retention characteristics of the floating-gate OFET memory devices.

The memory characteristics of the four floating-gate OFET memory devices demonstrated that the porous structure of PMMA film as tunneling layer was directly involved in the capture and release process of the charge when the floating-gate OFET memory devices was running. Moreover, when the thickness of PMMA tunneling layer of the floating-gate OFET memory devices was kept identical, the performance of the corresponding OFET memory devices was also improved as pore density of PMMA film increased. According to these results, we concluded that the porous structure of PMMA tunneling layer had positive impacts on device performance. The low and high density porous structure of PMMA films were characterized by the AFM, as shown in Fig. 1(c) and (d), respectively. The surface density of the pores of low and high density porous structure of PMMA film was estimated to 4 pC/μm^2 and 9 pC/μm^2, respectively. Thus the pore density of high density porous structure of PMMA film was more than twice that of low density porous structure of PMMA film. It was also calculated that pore average diameters of low and high density porous structure of PMMA film was 60 nm and 55 nm, respectively. And we also characterized the three-dimensional morphology of pentacene film on porous PMMA film by AFM, as shown in Fig. 5(a). The porous structure of pentacene film was also observed. These AFM images showed that pentacene grains penetrated into these pores of PMMA film during the thermal evaporation process which broadened the effective tunneling area between pentacene film and PMMA film. In order to obtain the clear evidence for the pentacene growth into the pores, the AFM images of pentacene film grown on nonporous and porous PMMA film were characterized, as shown in Fig. S1. Compared to the discrete pentacene grains of pentacene films grown on nonporous PMMA film, the porous structure was observed in the pentacene film grown on porous PMMA film, which was caused by pentacene grains penetrate into these pores of PMMA film during the thermal evaporation process. It is well-known that the charge passed through the tunneling layer by direct tunneling or Fowler-Nordheim (FN) tunneling in the floating-gate OFET memory devices [35]. For the direct tunneling and FN tunneling process of the floating-gate OFET memory devices, the number of the tunneling charge was closely related to the tunneling barrier between organic active layer and tunneling layer, that is, when the tunneling barrier reduced, more charge can overcome the tunneling barrier by direct tunneling and FN tunneling to participated in the memory process. When the tunneling area between pentacene film and PMMA film broadened,

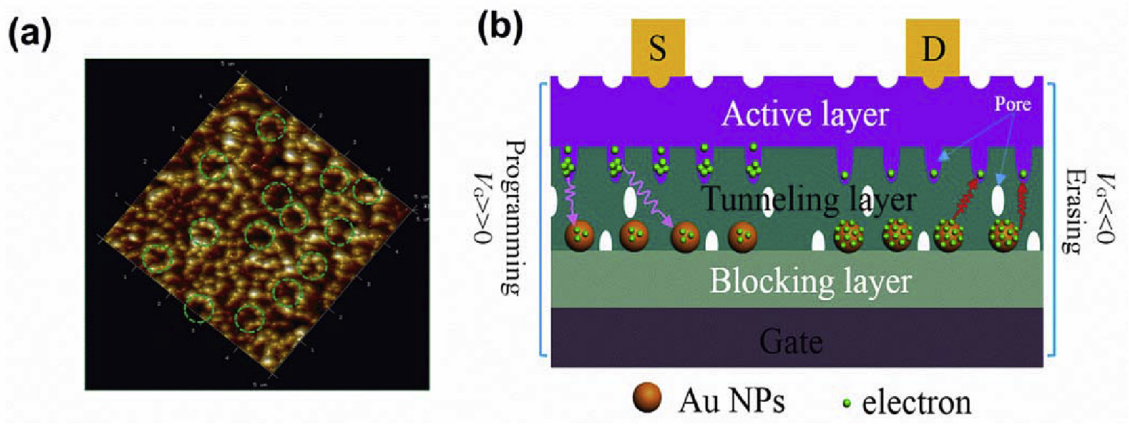

Fig. 5. (a) The AFM images of three-dimensional morphology of pentacene film on porous PMMA film. (b) The operational mechanism of porous structure of PMMA tunneling layer on the floating-gate OFET memory devices.

the electron tunneling probability also increased, which was equivalent to reduce tunneling barrier between pentacene film and PMMA film, in the case, more electrons could overcome the tunneling barrier and further captured/released by Au-NPs floating layer under the same programming/erasing voltage [26,36]. However, for the programming process, besides the number of tunneling charges, the shift of transfer curve during the programming process also was related to the capture charge capability of Au-NPs floating gate layer. Therefore, although the tunneling area between pentacene film and PMMA film broadened, the variation in the positive shift of transfer curve of the four OFET memory devices was approximately equal because the density and size of Au nanoparticles was identical in floating layer of the four OFET memory devices, as shown in Fig. 3(a)–(d). For the erasing process, when pore density of PMMA film increased, more trapped electrons could be released from Au-NPs floating layer to the conductive channel under the same erasing voltage, which resulted in the larger negative shift of transfer curve during the erasing process, as shown in Fig. 3(a)–(d). Eventually, the larger memory window was achieved in the OFET memory devices with high density porous structure of PMMA tunneling layer. On the other hand, as pore density of PMMA film increased, more electron transfer paths can be induced by the porous structure of PMMA tunneling layer under the programming/erasing voltage, thus the carrier concentration in the conductive channel of OFET memory devices can be maximally regulated during the programming/erasing process, which resulted in high ON/OFF current ratio during the endurance and retention process. Thus the capture and release efficiency of electron between the conductive channel and Au-NPs floating layer was enhanced due to the porous structure of PMMA tunneling layer, and correspondingly the endurance properties of the floating-gate OFET memory devices with porous structure of PMMA tunneling layer can be stably maintained. In addition, as shown in Fig. 1(c) and (d), the pore depth of low and high density porous structure of PMMA film was about between 5 nm and 8 nm, and the thickness of PMMA film was about 25 nm, so these pores didn't completely penetrate through the PMMA film. Compared to the hollow structure of PMMA film, the semi-hollow porous structure of PMMA film as tunneling layer had high insulating property, and it can also effectively block the electrons escape from Au-NPs floating layer to conductive channel during the programming process, which made the floating-gate OFET memory devices keep stable retention properties [26]. And the operational mechanism of porous structure of PMMA tunneling layer on the floating-gate OFET memory devices was shown in Fig. 5(b). Because of the above reason, the performance of floating-gate OFET memory devices can be improved by the porous structure of PMMA tunneling layer.

4. Conclusions

In conclusion, the floating-gate OFET memory devices based on thin/thick nonporous and low/high porous structure of PMMA film as tunneling dielectric layer were fabricated. Compared to the nonporous structure of PMMA tunneling layer, the device performance of the floating-gate OFET memory devices with the porous structure of PMMA tunneling layer can be effectively improved, the floating-gate OFET memory devices with high density porous structure of PMMA tunneling layer showed good nonvolatile memory effect including large memory window, high and stable ON/OFF current ratio of endurance and retention properties. The improvement of the floating-gate OFET memory devices with high density porous structure of PMMA tunneling layer was mainly attributed to both the high charge capture and release efficiency and the high electrical insulating property, which was caused by introducing the high density porous structure of PMMA film.

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Appendix A. Supplementary data

Supplementary data related to this article can be found at http://dx.doi.org/10.1016/j.orgel.2016.02.034.

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