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Analysis of temperature-dependent electrical transport properties of nonvolatile organic field-effect transistor memories based on PMMA film as charge trapping layer

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Abstract

The temperature-dependent electrical transport properties of nonvolatile organic field-effect transistor (OFET) memories with Poly (methyl methacrylate) (PMMA) as a charge trapping layer were characterized at four typical temperatures (20 °C, 60 °C, 80 °C and −78.5 °C). It was found that the OFET memories showed strong temperature dependence. The performance degradations, including the memory windows and the retention characteristics, could be observed at both high and low temperatures. The degradations of the OFET memories at 60 °C, 80 °C and −78.5 °C were attributed to both the less electrons trapped by the PMMA film and the easier release of the trapped electrons from the PMMA film, which is caused by the lower crystallinity of pentacene film and the larger contact area between pentacene film and PMMA film, respectively.

Keywords: nonvolatile memory, organic field-effect transistors, temperature dependent, surface morphology

S Online supplementary data available from stacks.iop.org/JPhysD/49/125104/mmedia

(Some figures may appear in colour only in the online journal)

1. Introduction

On account of the great potential in application, organic electronics have attracted tremendous attention. Considerable progress has been achieved in organic light-emitting diodes [1, 2], organic field-effect transistors (OFETs) [3, 4], and organic photovoltaic cells [5, 6], etc., making organic electronics much closer to practical use. As one of the important organic electronic devices, OFET memories are generally expected to be the promising candidates for the next generation memories, owing to their high storage density, nondestructive read-out, easily integrated structure and good compatibility with complementary oxide semiconductors [7–9]. So far, different types of OFET memories have been

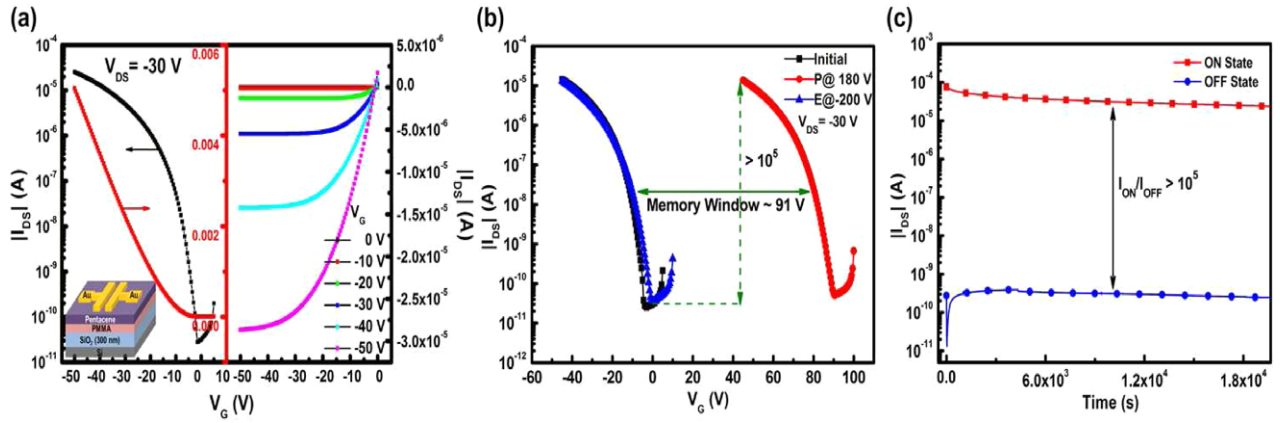

Figure 1. (a) Transfer (left) and output curves of the memories with PMMA as a charge trapping layer. (Inset) Device configuration of OFET memories with PMMA as an electret layer. (b) Programming and erasing characteristics with programming voltage ($V_G = 180$ V, $V_{DS} = -30$ V) and erasing voltage ($V_G = -200$ V, $V_{DS} = -30$ V). (c) The retention time of the saturation current at ON and OFF states.

demonstrated such as floating-gate OFET memories [10, 11], polymer electret OFET memories [12, 13] and ferroelectric OFET memories [14]. Many efforts have been devoted to improving the performance of the OFET memories at room temperature, including memory window, on/off current ratio, endurance and retention properties [15–18], etc. However, memory performance could be affected by the operation temperature [19–21], which is an unavoidable issue to achieve the practical application. Although many studies have been conducted to investigate the thermal stability of the OFETs [22–24], the investigation on the temperature-dependent electrical transport properties of the memories based on OFETs is still limited, and the corresponding mechanism of the temperature-dependent effect on the memory performance remains unclear. In addition, there are some temperature requirements for the data storage and operation of thin-film memories. It is usually expected that the temperature ranges of storage and operation are −40 °C to 85 °C and −20 °C to 50 °C [25], respectively, but most researchers mainly focused on the effect of high temperature on device performance while neglecting the effect of low temperature, which is insufficient to comprehensively understand the electrical transport properties of these memories. Since the charge transport and storage process of the OFET memories strongly depend on the following factors: (i) the properties of charge trapping layer, source/drain electrodes and organic active layer [13]; (ii) the interfaces including source-drain electrodes/organic active layer interface and organic active layer/charge trapping layer interface [26]. Therefore, a detailed study would contribute to fully understanding the origin of the temperature dependence of OFET memories.

In the paper, we studied the temperature-dependent electrical transport properties of the OFET memories using PMMA film as a charge trapping layer at four different temperatures (20 °C, 60 °C, 80 °C and −78.5 °C). In order to investigate the influence of the temperature effect on the memory performance of OFET memories, the pentacene film, the PMMA film, both Au/pentacene interface and pentacene/PMMA interface were analyzed by atomic force microscope (AFM), x-ray diffraction (XRD) and ultraviolet photoelectron spectroscopy (UPS), respectively. Meanwhile, the mechanism on the thermal stability of the OFET memories was discussed in detail.

2. Experimental

The OFET memories were fabricated in bottom-gate and top-contact configuration, as shown in the inset of figure 1(a). All the devices were fabricated on the heavily-doped Si wafer which served as the gate electrode with 300 nm-thick thermally grown SiO_2 on top. The substrates were cleaned in an ultrasonic bath with acetone and isopropanol for 5 min, respectively, and then dried in the oven at 100 °C after rinsing with deionized water. After the standard cleaning, the polymer electret layer was deposited on the SiO_2/Si substrate by spin-coating PMMA (Sigma-Aldrich, weight-average molecular weight $M_W = 12\,000$) solution (in toluene) at 3000 rpm for 1 min. Subsequently, the substrates were transferred in the oven to bake for 1 h at 100 °C in the air. After that, pentacene was deposited by thermal vacuum evaporation, which was employed as the active channel layer. Finally, the devices were completed by the formation of Au source and drain electrodes through the metal shadow mask, of which the channel length (L) and channel width (W) were 100 um and 2000 μm, respectively. The electrical characteristics of the OFETs memories were measured with an Agilent B1500A semiconductor parameter analyzer under ambient conditions without any encapsulation. For the experiment focusing on the stability under high temperatures, the prepared devices were measured at 60 °C and 80 °C, respectively. For the experiment focusing on the stability under low temperature, the prepared device was put upon a glass petri dish that was filled up with dry ice, and the memory characteristics were measured under such low temperature condition. The thicknesses of Au, pentacene and PMMA films were measured by a Bruker Dektak XT stylus profiler and estimated to be 20 nm, 50 nm and 9.87 nm, respectively. The total capacitance for PMMA and SiO_2 is 11.1 nF cm^{-2}. AFM was carried out with a Bruker Scan Asyst to analyze the surface morphology and roughness of the pentacene films and PMMA films. The crystal structures of the

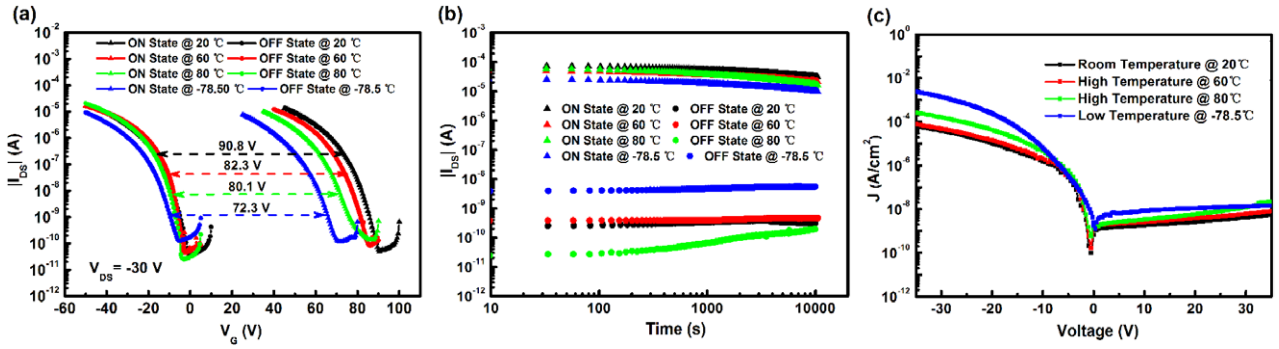

Figure 2. (a) Programming and erasing characteristics with programming voltage ($V_G = 180$ V, $V_{DS} = -30$ V) and erasing voltage ($V_G = -200$ V, $V_{DS} = -30$ V) at four different temperatures (20 °C, 60 °C, 80 °C and −78.5 °C). (b) Retention characteristics at four different temperatures (20 °C, 60 °C, 80 °C and −78.5 °C). (c) Gate leakage current at four different temperatures (20 °C, 60 °C, 80 °C and −78.5 °C).

pentacene films were investigated by using XRD (Bruker D8 advance). UPS was used for the measurement to the energy barrier between Au electrodes and the pentacene film, using a helium discharge lamp (Hel $\alpha = 21.2$ eV) and a hemispherical energy analyzer (Specs PHOIBOS 150).

3. Results and discussion

Figure 1(a) shows the representative output and transfer characteristics of the OFET memories based on PMMA electrets at 20 °C. The memories showed typical p-type OFET behavior with obvious linear regime at lower source-drain voltage (V_{DS}) and saturation regime at higher V_{DS}, which indicated that holes were well accumulated in the conductive channel in the pentacene layer near the interface between the pentacene film and the PMMA electret layer. From the transfer curve, the carrier mobility (μ), threshold voltage (V_{th}) and ON/OFF current ratio were calculated to be 0.4 cm^2 $V^{-1}s^{-1}$,−14.6 V and 10^6, respectively. Figure 1(b) shows the programming and erasing characteristics of the OFET memories at 20 °C. With the application of programming and erasing voltages at 180 V and −200 V for 1 s, respectively, the measured memory window was approximate 91 V when the V_{DS} was kept at −30 V. The memory window of the OFET memories was attributed to the trapping and de-trapping of the electrons in the PMMA electret layer, which was consistent with the memory mechanism of the previous reports [9, 27]. Figure 1(c) shows the retention characteristics of the OFET memories at 20 °C. The retention time was measured at $V_G = 0$ V which could avoid the instability caused by the gate bias stress and meanwhile reduce the electrical consumption of the devices. The retention time could be well maintained for at least 10^4 s with a high on/off current ratio of over 10^5, showing that the OFET memories at 20 °C had stable data storage capacity. The above electrical characteristics demonstrated that the OFET memories based on PMMA as a charge trapping layer had reliable memory performance at 20 °C, which were ideally suited to investigating the electrical transport properties of the OFET memories under different temperatures.

To study the temperature-dependent electrical transport properties of the OFET memories based on PMMA, we measured the electrical characteristics of the devices at high temperatures of 60 °C and 80 °C, and at a very low temperature of −78.5 °C. Figure 2(a) shows the programming and erasing characteristics of the OFETs memories at four different temperatures (20 °C, 60 °C, 80 °C and −78.5 °C). When a programming voltage of 180 V was applied to the memories for 1 s with V_{DS} maintained at −30 V, the transfer curves of the OFET memories at four different temperatures all shifted to the positive direction. However, the shift in the transfer curve at 20 °C was more than that at 60 °C, 80 °C and −78.5 °C, meaning that more electrons were trapped by the PMMA electret layer during the programming process at room temperature as compared to at 60 °C, 80 °C and −78.5 °C. After applying an erasing voltage of −200 V for 1 s to the memories, the transfer curves of these OFET memories substantially returned closely to their initial states, which meant that those electrons trapped by the PMMA electret layer at four different temperatures all could be released and further combined with holes in the conductive channel. As a result, the different memory windows of the OFET memories at four different temperatures were obtained under the same programming/erasing voltage, which were 90.8 V (20 °C), 82.3 V (60 °C), 80.1 V (80 °C) and 72.3 V (−78.5 °C), respectively. Figure 2(b) shows the retention characteristics of the OFET memories at four different temperatures (20 °C, 60 °C, 80 °C and −78.5 °C). Compared to the ON states, the OFF states of the OFET memories exhibited stronger temperature dependence. The OFF states currents at 80 °C and −78.5 °C showed much more degradation than that of the memories at 20 °C, showing that the trapped electrons in the PMMA electret layer at 80 °C and −78.5 °C were very difficult to preserve and easily released under the same erasing voltage, while OFF state characteristics of the memories at 60 °C were quite stable, which was similar to the devices at 20 °C. In addition, the OFF state current at −78.5 °C was increased by more than one order of magnitude than at 20 °C, while the OFF state current at 80 °C was decreased by almost one order of magnitude than at 20 °C. To demonstrate the operating stabilities and reliabilities of the OFET memories at different temperatures, the bias stress on the OFETs at four different temperatures was measured [28], as shown in figure S1 (stacks.iop.org/JPhysD/49/125104/mmedia) in the supporting information. We also measured the transfer characteristics before and after

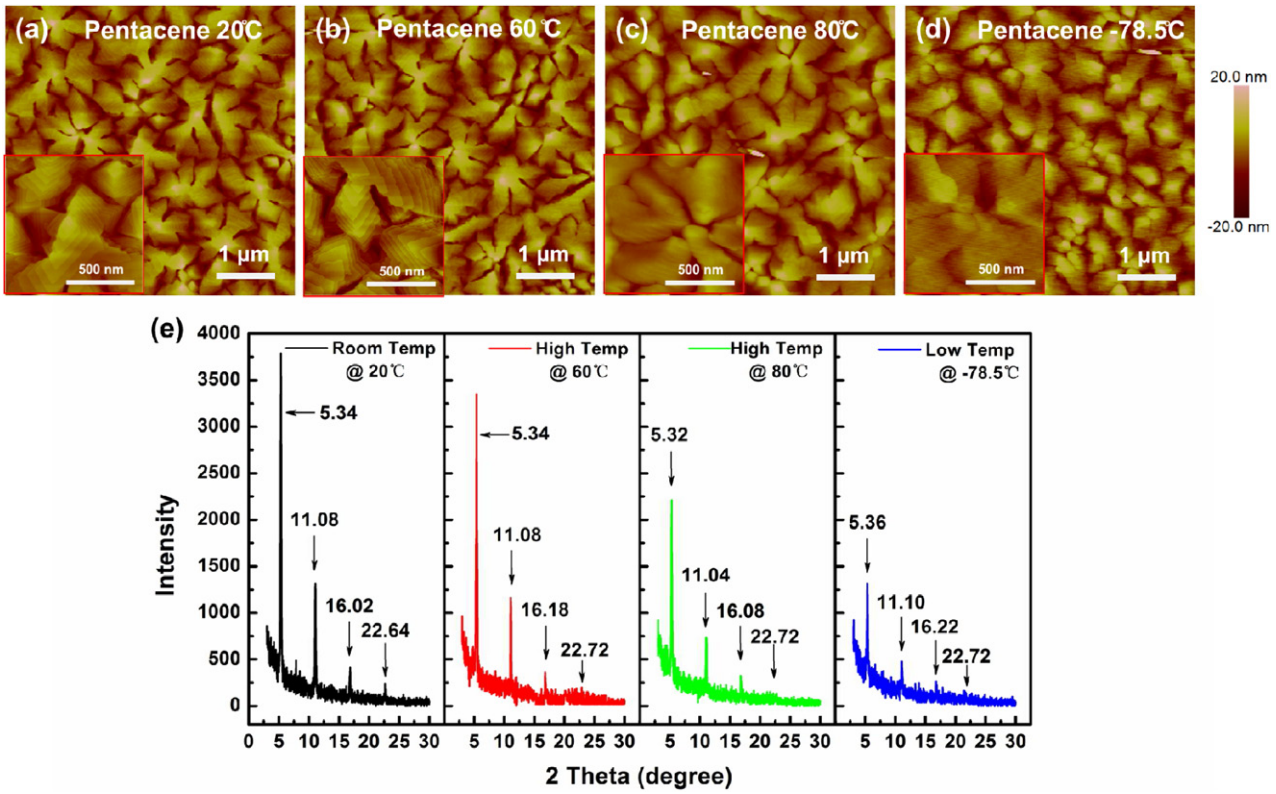

Figure 3. AFM images (5 μm × 5 μm) of pentacene thin films on PMMA layers after thermal annealing at (a) 20 °C, (b) 60 °C, (c) 80 °C and (d) −78.5 °C. The insets show the corresponding 1 μm × 1 μm AFM images. (e) X-ray diffraction patterns of pentacene thin films after thermal annealing at 20 °C, 60 °C, 80 °C and −78.5 °C. The thickness of the pentacene was 50 nm.

the retention time and several switching cycles for each device, as shown in figures S2 and S3, respectively. In these two cases, the shifts of V_{th} were relatively small compared to the large memory window of the OFET memories, showing that the OFET memories have high operating stabilities and reliabilities. Figure 2(c) shows the characteristics of gate leakage currents at different temperatures. For the devices measured at positive temperatures (20 °C, 60 °C and 80 °C), the current densities increased with the increase of temperatures, which agreed well with the results about the thermal conductivity of PMMA in the previous reports [29]. However, the device at −78.5 °C showed the highest current density among these devices at different temperatures, which was not consistent with the variation trend. It should be noticed that our devices were measured in the ambient air, so the effect of oxygen and humidity should be considered. It has been demonstrated that pentacene OFETs are more sensitive towards humidity than oxygen [30]. In our experiments, the humidity (RH) of the ambient air was kept at 16–18%. Such humidity (<20%) had less effect on the devices measured at positive temperatures, but the humidity significantly increased on the device surface and further affected the devices measured at low temperature by diffusing into the grain boundaries of pentacene, leading to a high OFF state current [31, 32]. In contrast to the OFF states, the ON states of the OFET memories at four different temperatures showed a similar degradation tendency, meaning that the programming process would not be easily affected by the temperature effect. Therefore, we believe that the performance degradation of the OFET memories at the high and low temperatures was attributed to the less electrons trapped by the PMMA electret layer, easier release of the trapped electrons from the PMMA electret layer which were caused by the temperature effect as well as the humidity effect.

In order to investigate the influence of the temperature effect on the charge trapping and de-trapping process, AFM images of 50 nm pentacene film grown on PMMA/SiO_2/Si substrate at four different temperatures (20 °C, 60 °C, 80 °C and −78.5 °C) were characterized, as shown in figure 3. The pentacene films at both 20 °C and 60 °C were composed of grains with distinct terraces, which indicated the pentacene films of higher crystallinity, as shown in figures 3(a) and (b). However, the terraces of the grains, which were composed of pentacene films, became vague at 80 °C, and even completely disappeared at −78.5 °C, as shown in figures 3(c) and (d), respectively. We considered that the decrease in the crystallinity of pentacene films at 80 °C was mainly attributed to the thermal degradation, while the decrease in the crystallinity of pentacene films at −78.5 °C resulted from the thermally-induced humidity effect. The crystallinity of pentacene films at four different temperatures were further confirmed by XRD, as shown in figure 3(e). The XRD spectra of pentacene films at four different temperatures all appeared as a series of patterns with (00k) peaks. High intensities can be observed at $2\theta = 5.34 \pm 0.02°$, which diffracted from the thin-film phase of pentacene films [33, 34], showing that the crystalline structure of pentacene films was not affected by the temperature effects. However, the diffracted intensities of pentacene films at 60 °C, 80 °C and −78.5 °C were lower than that at 20 °C, the

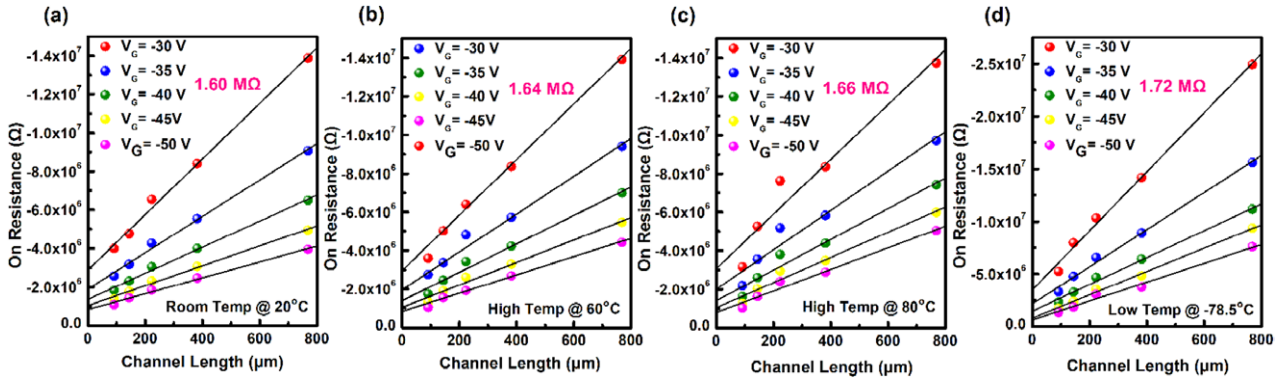

Figure 4. Plot of On resistance versus channel length for OFET memories with PMMA as a charge trapping layer at (a) 20 °C, (b) 60 °C, (c) 80 °C and (d) −78.5 °C. The value of gate voltages varies from −30 V to −50 V in steps of 5 V.

variation of the diffracted intensity of pentacene films at four different temperatures was basically consistent with the terrace's clarity of pentacene grains shown by the AFM images, further demonstrating that the crystallinity of pentacene films at 80 °C and −78.5 °C were lower than that at 20 °C and 60 °C. From the AFM and XRD results, it can be concluded that both the high temperature effect as well as the humidity effect resulting from low temperature had direct influences on the crystallinity rather than the crystal structure of pentacene films, and the crystallinity of pentacene films would decrease when the pentacene-based OFET memories were at both high and low temperatures. The lower crystallinity of pentacene films could generate a higher density of physical defects in the pentacene films, the Au/pentacene and the pentacene/PMMA interface, which could significantly affect charge injection, charge trapping and de-trapping during the memory process. Therefore, we believe that the performance degradations of the OFET memories at the lower and higher temperatures were related to the decreased crystallinity of pentacene films.

To further understand the effect of pentacene film crystallinity on the performance of the OFET memories, we measured the value of the total resistance on channel length of OFET memories at four different temperatures (20 °C, 60 °C, 80 °C and −78.5 °C), and the contact resistance (R_C) between Au electrodes and pentacene films was obtained from the intercept by extrapolating the resistance line at various gate voltages (V_G) to the zero channel length, as shown in figure 4. The R_C of the OFET memories at four different temperatures (20 °C, 60 °C, 80 °C and −78.5 °C) were 1.60 MΩ (20 °C), 1.64 MΩ (60 °C), 1.66 MΩ (80 °C) and 1.72 MΩ (−78.5 °C), respectively. The variation of the R_C matched well with the crystallinity of pentacene films at four different temperatures, that is, the R_C increased as the crystallinity decreased. It was well known that the R_C of the OFETs was related to both the interface and the energy barrier between the source/drain electrodes and organic semiconductor layers [35]. The UPS spectra was measured to study the energy barrier between Au electrodes and pentacene films at four different temperatures (20 °C, 60 °C, 80 °C and −78.5 °C), as shown in figure S4 of the supplementary information. From the UPS spectra, the energy barrier between Au electrodes and pentacene films at four different temperatures remained unchanged. Therefore, it can be concluded that the variation of the R_C was mainly caused by the interface between Au electrodes and pentacene films which was affected by the crystallinity of pentacene films. As the crystallinity of pentacene films decreased, it would generate a high density of physical defects at the interface between Au electrodes and pentacene films which increased the R_C, leading to a decrease in the hole-injection ability from Au electrodes to pentacene films. Thus the number of the electrons induced by the injected holes also reduced in the conductive channel between the pentacene film and the PMMA layer. As a result, compared to the OFET memories at 20 °C, less electrons were trapped by PMMA layers in the OFET memories at 60 °C, 80 °C and −78.5 °C during the programming process, resulting in smaller shifts of the transfer curves under the same programming voltage.

For the charge trapping OFET memories, the process of charge trapping and de-trapping mainly occurred between the active layer and the electret layer, so it was necessary to research the variation in their interfaces at different temperatures. The AFM images of 10 nm-thick pentacene film grown on PMMA/SiO_2/Si substrate at four different temperatures (20 °C, 60 °C, 80 °C and −78.5 °C) were measured, as shown in figures 5(a)–(d). It can be seen that there was no appreciable difference in the morphologies of 10 nm-thick pentacene films at high temperatures, and their films were composed of grains with distinct terraces, as shown in the insets of figures 5(a)–(d). However, compared to pentacene film at 20 °C, the root-mean-square (rms) roughness of pentacene films at 60 °C and 80 °C exhibited decreases from 2.31 nm to 2.29 and 2.25 nm, respectively. The pentacene film at −78.5 °C showed different morphology, which consisted of very vague pentacene grains due to high humidity, and its corresponding rms roughness also decreased to 2.14 nm. Figures 5(e)–(h) show the AFM images of PMMA film grown on SiO_2/Si substrate at four different temperatures (20 °C, 60 °C, 80 °C and −78.5 °C), and the corresponding 3D AFM images of PMMA film are shown in figures 5(i)–(l). Compared to the PMMA film at high temperatures, the morphology of PMMA film at −78.5 °C obviously changed, and many small projections formed on the surface. Meanwhile, the rms roughness of PMMA film at four different temperatures was estimated to be 0.266 nm (20 °C), 0.266 nm (60 °C), 0.273 nm (80 °C) and 0.277 nm (−78.5 °C), respectively. In view of the AFM results of 10 nm-thick pentacene films, it was found that the rms

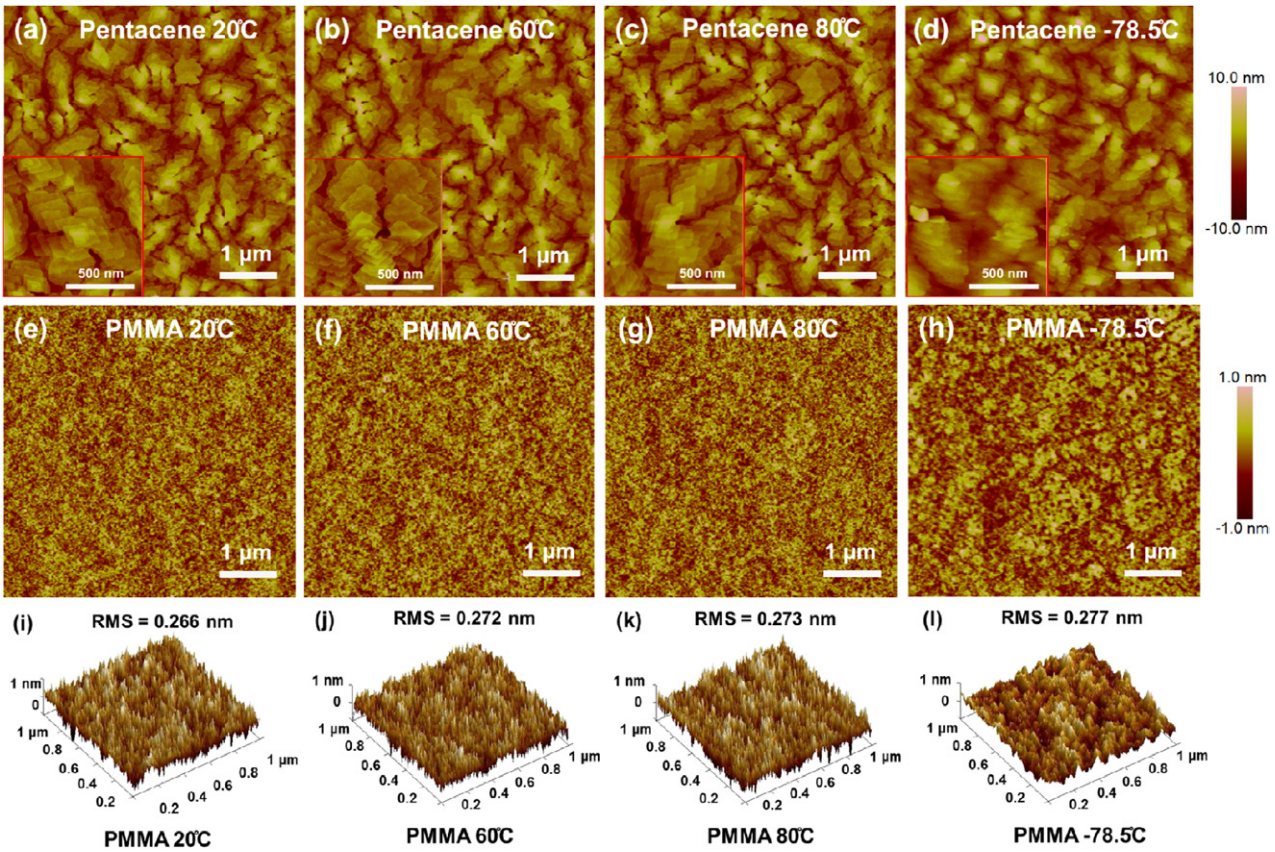

Figure 5. AFM images (5 μm × 5 μm) of 10 nm-thick pentacene films on the PMMA layer after thermal annealing at (a) 20 °C, (b) 60 °C, (c) 80 °C and (d) −78.5 °C. The insets show the corresponding 1 μm × 1 μm AFM images. AFM images (5 μm × 5 μm) of the PMMA layer after thermal annealing at (e) 20 °C, (f) 60 °C, (g) 80 °C and (h) −78.5 °C. 3D AFM images (1 μm × 1 μm) of the PMMA layer after thermal annealing at (i) 20 °C, (j) 60 °C, (k) 80 °C and (l) −78.5 °C.

variation of pentacene films was opposite to that of the PMMA films at four different temperatures, which was mainly caused by the lower crystallinity of pentacene films on the rougher surface of PMMA film. Meanwhile, combined with the 3D AFM images of pentacene films and the PMMA films at four different temperatures (20 °C, 60 °C, 80 °C and −78.5 °C), we can assume that the contact areas between pentacene films and PMMA films at 60 °C, 80 °C and −78.5 °C were larger than that at 20 °C, which made it easier for charge transfer from PMMA films to pentacene films. That is, it was difficult to preserve the trapped electrons in the PMMA film due to the larger contact area, and the trapped electrons in the PMMA film could be more easily released and transferred to the pentacene film under the same erasing voltage which resulted in more retention degradation in OFF states of OFET memories at 80 °C and −78.5 °C than that of OFET memories at 20 °C.

4. Conclusions

The temperature-dependent electrical transport properties of the OFET memories based on PMMA as a charge trapping layer were investigated at four different temperatures (20 °C, 60 °C, 80 °C and −78.5 °C). It was found that the OFET memories at both high and low temperatures showed degradations on memory performance compared to the devices at 20 °C. The high gate leakage current at low temperature indicated that the devices may be affected by the humidity in ambient air. The AFM and XRD of pentacene films and PMMA films at four different temperatures revealed that the origins of the performance degradations of the OFET memories at both high and low temperatures were attributed to the lower crystallinity of pentacene film and the larger contact area between pentacene film and PMMA film, which resulted in less electrons being trapped by the PMMA film and an easier release of the trapped electrons from the PMMA film, respectively.

Acknowledgments

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